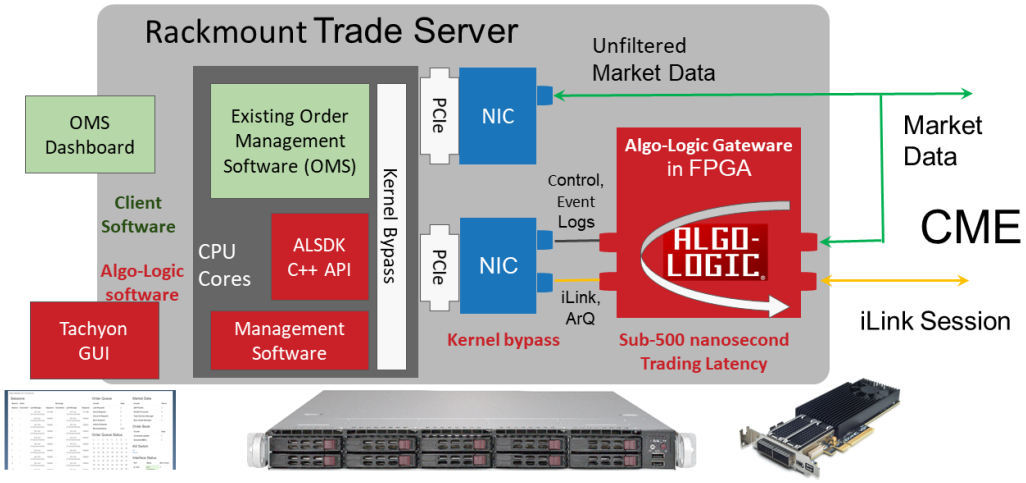
FPGA Accelerated CME Tick-To-Trade System With HLS & Turbo Spreader



Description

Algo-Logic Systems' 5th generation FPGA accelerated Gateware Defined Networking® (GDN) CME Tick-To-Trade (T2T) System is a sub-500 nanosecond trading solution. It supports all CME Group exchanges including CBOT, COMEX, and NYMEX. The solution is built using Algo-Logic Systems' internally developed, pre-built IP cores that significantly reduce time-to-market and provide flexibility for customizations.

Sub-microsecond wire-to-wire latencies are achieved by receiving CME MDP 3.0 tick data directly into the FPGA on a 10G link, detecting opportunities by building order books, and placing trades in form of FIX messages encapsulated in TCP packets using the ultra-low latency (ULL) 10G TCP Endpoint.

The CME T2T system includes parametrized triggers for mass quote cancel, mass action request and fast arbitrage as well as the ability to modify FIX order fields in FPGA logic. It integrates with existing Order Management Systems (OMS) through C++ Application Programing Interfaces (APIs). A Graphical User Interface (GUI) and RESTful APIs are provided for control and monitoring of the accelerator.

ArQ C++ Library and API:

- Low latency C++ 98 compatible APIs are used to set up triggers and preload FIX orders to be injected
- Well defined API to pass trigger parameters between hardware and software

Control Software includes:

- Device parameter configuration (i.e., IP and MAC addresses) and status monitoring
- Logging and event notifications

FPGA-Accelerated Trading

- **Quote Cancellation**
  - Ultra-low-latency mass quote cancellation by product, instrument group or each instrument
- **On Fill Trigger**
  - Instantly reacts to market data or order fill, whichever comes first, to trigger response order(s)
- **Turbo Spreading**
  - Auto-reload enables multiple hedges and quotes to be sent using pre-loaded FIX order
  - Allows trading on multiple instruments with simultaneous multi-leg strategies
  - Supports hardware trading strategies in logic
- **HLS Triggers**
  - High-level synthesis allows customers to implement custom triggers to support their proprietary strategies
  - Allows trigger inputs from Market Data, Customer generated parameters, Top of Book, and incremental updates

Short Time to Market

Algo-Logic's prebuilt IP cores with sub-microsecond latency

- ULL 10GE PHY+MAC
- CME Feed Handler
- CME Futures & Options Order Book
- 10G TCP Endpoint
- FIX Message Processing

Augments existing Order Management Systems

- Minimal changes to software through well-defined APIs
- No FPGA programming skills required

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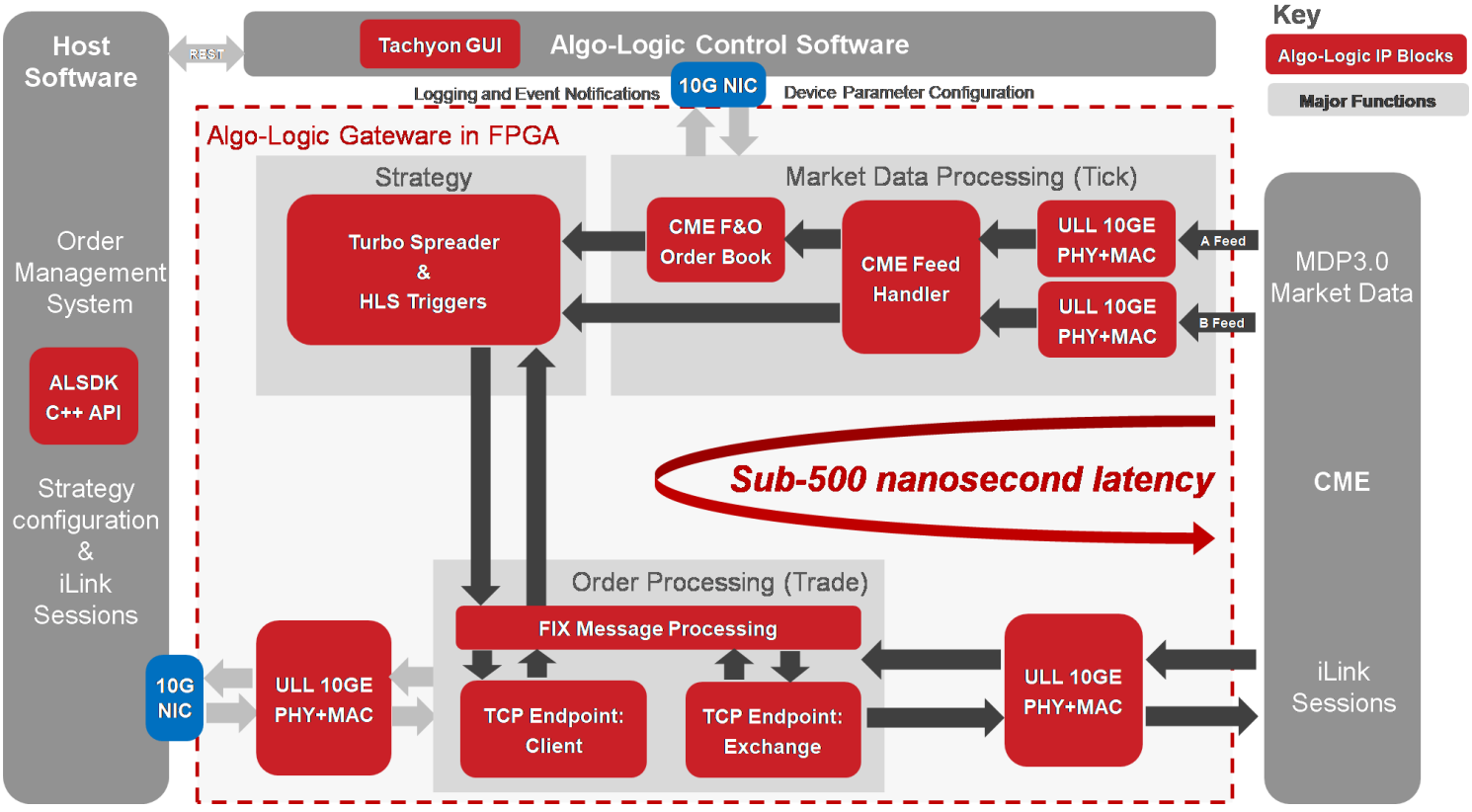
CME Tick-To-Trade System Features and Base Specifications

FPGA Accelerated Trading	Multi-leg turbo spreading, quote cancel, and on fill triggers
Pre-Built IP Cores	CME Feed Handler, CME Futures & Options Order Book, 10G TCP Endpoint, ULL 10GE PHY+MAC
Multicast Channels for Market Data	Up to 16
Order Book Configuration	20 security IDs with L2 snapshots containing BBO, all 10 book levels
FIX Sessions and Order Queues	32 and 64 respectively, with 2 Kbyte per queue message size limit
Turbo Spreading in Logic	Fast arbitrage across multiple legs
Configurable Number of lean Legs	2 with full support for quoting one or two legs of a spread or strategy
Logging and Event Notifications	FIX logs, Raw Market Data logs, CME Order Book BBO, Trigger events
FPGA Device and Platform	Xilinx UltraScale+ with 10 Gbps Ethernet on Exablaze ExaNIC V5P

CME Tick-To-Trade System Diagram



Algo-Logic Systems builds FPGA accelerated Gateware Defined Networking® (GDN) latency.

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